METHOD AND SYSTEM FOR MINIMIZING MEMORY CORRUPTION

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BACKGROUND

[0001] Field of the Invention

[0002] The present invention relates to host bus adapters, and more particularly, to minimizing corruption of memory used by host bus adapters.

[0003] Background of the Invention

[0004] A Host bus adapter (may also be referred to as "controller", "adapter" or "HBA") is an adapter placed between a host system computer bus and a network (fibre channel system, Ethernet, Gigabit Ethernet, or any other system). HBAs manage transfer of information between the host system and the network. To minimize the impact on host processor performance, HBAs perform various interface functions automatically or with minimal host processor involvement.

[0005] HBAs are connected to a host system via standard buses. One such bus is the Peripheral

Component Interconnect ("PCI"), a standard bus developed by Intel Corporation®, incorporated herein by reference in its entirety. PCI is a 64-bit bus, though it is usually implemented as a 32-bit bus. It can run at clock speeds of 33 or 66 MHz. At 32 bits and 33 MHz, it yields a throughput rate of 133 MBps.

[0006] PCI-X is another standard bus that is backward compatible with existing PCI cards. The PCI-X standard is incorporated herein by reference in its entirety. PCI-X improves upon the speed of the PCI bus from 133 MBps to as much as 1 GBps. PCI-X was designed to increase performance of high bandwidth devices, such as Gigabit Ethernet and Fibre Channel.

[0007] Most HBAs are coupled to non-volatile random access memory ("NVRAM") that allows HBAs to move information from a host and to /from the network. The problem with conventional HBAs using NVRAM is that the NVRAM may be erased accidentally when the HBA is powered on.

[0008] Typically, NVRAM control inputs are driven by general-purpose input/out ("GPIO") pins from an HBA (or any other integrated circuit), which interfaces with a host system through a PCI

backplane. At power up, and even sometimes during reset of the HBA, PCI backplanes drive noisy and non-deterministic waveforms on the RESET pin of the HBA. The GPIO pins can also drive unpredictable waveforms due to the PCI RESET behavior. One such waveform may issue an "ERASE" command to the NVRAM that erases NVRAM content.

[0009] As HBAs are being deployed in modern networks, with high bandwidth and performance requirements, such accidental erasure of information can be devastating to the overall performance of computing systems.

[00010] Therefore, what is needed is a method and system for preventing corruption of NVRAM information during power-up and/or reset.

[00011] SUMMARY OF THE INVENTION

[00012] In one aspect of the present invention, a system for minimizing memory (which includes NVRAM) corruption at power up and/or reset is provided. The system includes, a potentiometer/variable resistor between an adapter and the memory; and a voltage divider functionally coupled to the potentiometer. The voltage divider includes a pull-down resistor that brings down the voltage at one of the plural

potentiometer pins, minimizing the chances of memory corruption.

[00013] The potentiometer is driven by signals from the adapter and is in increment/decrement mode upon power up and/or reset. The potentiometer includes a wiper, which is stepped by an input up/down signal from the adapter.

[00014] In another aspect of the present invention, a method for minimizing memory corruption at power up and/or reset is provided. The method includes, setting a potentiometer/variable resistor to a resistance value such that upon power up and/or reset data cannot be written to the memory; and setting the potentiometer in a decrement/increment mode such that resistance between plural pins of the potentiometer can be decreased/increased allowing content to be written to the memory after power up and/or reset.

[00015] In yet another aspect of the present invention, a circuit for minimizing memory corruption at power up and/or reset is provided. The circuit includes, means for setting a potentiometer/variable resistor to a resistance value such that upon power up and/or reset, data cannot be written to the memory; and means for setting the potentiometer in a decrement mode such that resistance between plural pins of the

potentiometer can be decreased allowing content to be written to the memory after power up and/or reset.

[00016] In one aspect of the present invention, writing to NVRAM is disabled during power-up and/or reset. Thereafter, writing to NVRAM is enabled. This minimizes the chances of accidental erasure during power up and/or reset.

[00017] This brief summary has been provided so that the nature of the invention may be understood quickly. A more complete understanding of the invention can be obtained by reference to the following detailed description of the preferred embodiments thereof concerning the attached drawings.

[00018] BRIEF DESCRIPTION OF THE DRAWINGS

[00019] The foregoing features and other features of the present invention will now be described with reference to the drawings of a preferred embodiment. In the drawings, the same components have the same reference numerals. The illustrated embodiment is intended to illustrate, but not to limit the invention. The drawings include the following Figures:

[00020] Figure 1 shows a block diagram of a typical storage area network;

[00021] Figures 2A-2B show block diagrams of an HBA used according to one aspect of the present invention

[00022] Figure 3 shows a schematic to minimize NVRAM corruption, according to one aspect of the present invention; and

[00023] Figure 4 is a flow diagram of executable process steps for minimizing NVRAM corruption, according to one aspect of the present invention.

[00024] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00025] To facilitate an understanding of the preferred embodiment, the general architecture and operation of a system using HBAs will be described. The specific architecture and operation of the preferred embodiment will then be described with reference to the general architecture.

[00026] Figure 1 shows a typical storage area network 100 with host systems 102, 104, 107 and 109 coupled to various disks 103, 105, 106 and 108 via network 101. Host system 104 (or others) are not described in detail, but it includes a central processing unit (CPU), a system memory (typically, random access memory "RAM"), read only memory (ROM) coupled to a system bus and a DMA controller unit. Host system 104 may be functionally coupled to an HBA using a PCI interface.

[00027] Figure 2A shows a top-level block diagram of system 200 using an adapter (or HBA) 200A on

a field programmable array ("FPGA") board. Adapter 200A includes an embedded processor 202 (which may include more than one processor) and a TCP/IP accelerator 204 that implements the TCP/IP protocol in hardware for processing network packets 210 that are received by a gigabit interface converter ("GBIC") 207. GBIC 207includes a transceiver for converting serial electric signals to serial optical signals and vice-versa. This is used to interface with a fiber optic/Ethernet system (Fibre Channel and Gigabit Ethernet systems).

[00028] Serial/de-serializer 206 serializes or de-serializes the signals before they enter (or leave) adapter 200A.

[00029] PCI interface 203 allows adapter 200A to interface with a host system (for example, host system 104).

[00030] Programmable random access memory ("RAM") 201 is provided to adapter 200A for executing firmware commands.

[00031] System 200A is coupled to NVRAM 205 via a digital potentiometer (also referred to herein as "digital pot") 208. NVRAM 205 may be a serial programmable read only, and write

enabled memory. In this example, NVRAM 205 may be M93S66 ™ as sold by ST Micro ™ or FM93CS66 ™ sold by Fairchild Semiconductor Corporation ™. It is noteworthy that the adaptive aspects of the present invention are not limited to any particular type/model/size of NVRAM.

[00032] Digital pot 208 receives input via GPIO pins 209, according to one aspect of the present invention, as described in detail below. The term digital potentiometer as used throughout this specification means digitally controlled potentiometers that include variable resistors and traditional potentiometers. Various companies market digital potentiometers that can be configured both as a variable resistor or potentiometer. One such digital pot 208 is MAX5464, 50 k-ohm variable resister (sold as 32-Tap FleaPot™, 2 Wire Digital Potentiometer), marketed by Maxim Semiconductor®. Some other companies that market digital potentiometers are Microchip Corporation, Analog Devices Inc. and Xicor Inc. It is noteworthy that the adaptive aspects of

the present invention are not limited to any particular brand or rating of digital pot 208.

[00033] System 200A is powered on by power module 211, which can be internal or external to system 200A. The adaptive aspects of the present invention are not limited to any particular power supply module.

[00034] Figure 2B shows an application specific integrated circuit ("ASIC") implementation of the system described above with respect to Figure 2A. System 200B is similar to system 200A, except in this case it is an ASIC. System 200B is coupled to a host system via a PCI-X interface 203A. RAM 201 and SERDES 206 are on board (integrated in ASIC 200B). Most of the components in system 200B and 200A have the same functionality.

[00035] It is noteworthy that the foregoing systems are not intended to limit the present invention. Any adapter that uses an NVRAM or similar memory can use the various aspects of the present invention.

[00036] Figure 3 shows a circuit diagram of system 300, according to one aspect of the present invention, that prevents erasure of NVRAM 205 on power up and/or reset of system 200A and/or 200B. For illustration

purposes, ASIC as referred herein with respect to Figure 3, includes systems 200A and/or 200B.

[00037] Digital pot 208 receives various inputs from system 200B, including, input 301, which is used to control the up/down ("U/D") pin (i.e. toggle pin 3 of digital pot 208). Another input 302 is used to control the chip select (also referred to as "CS") (pin 4 of digital pot 208). Input 302 addresses digital pot 208 and enables resistance change, as described below.

[00038] Digital pot 208 receives input voltage at pin 1 (Vdd 304) and is grounded at pin 2 (303). To illustrate one aspect of the present invention, Vdd may be 3.3V. It is noteworthy that the adaptive aspects of the present invention are not limited to any particular voltage at pin 6 or pin 1.

[00039] Resistor R1 305 acts as a "pull down" resistor forming a voltage divider with digital pot 208 pin L (i.e. pin 5). To illustrate one aspect of the present invention, R1 305 may be 4.7K. It is noteworthy that the adaptive aspects of the present invention are not limited to any particular resistance value of R1 305.

[00040] NVRAM 205 receives signals 308-310 from system 200B. Signal 308 is a clock signal, signal 309 is a chip select signal and signal 310 is a "data-in" signal that allows data content to be written in NVRAM

205. The foregoing signals allow system 200B to access NVRAM 205.

[00041] NVRAM receives signal 306 (EE_PE) that enables system 200B firmware to write to NVRAM 205.

[00042] At power on of system 200B, digital pot 208 is set somewhere in the mid-point of its resistance range. In the foregoing illustration, that will be around 25K-ohm value, which will be the resistance between pin 6 and 5 of digital pot 208. At power up, R1 305 forms a voltage divider, and voltage at pin 5 of digital pot 208 is given by:

[00043] Vdd * (R1/(R1 + R2)), where R1 is resistor 305 and R2 is the resistance of the digital pot 208 at power up (in the foregoing example, 25 K-ohm). If Vdd is 3.3V and R1 305 is 4.7K-ohm, the voltage at pin 5 of digital pot 208 is 0.16Vdd, i.e. 0.52V. This voltage or voltage similar to this is applied to pin 6 of NVRAM 205. This disables the ability to write to NVRAM 205.

[00044] To enable writes, firmware running on system 200B drives GPIO pins (signals 301 and 302) to decrease the resistance between pins 5 and 6 of digital pot 208. Firmware commands digital pot 208 to change resistance a certain way (i.e. up or down) by driving signals 301 and 302. When signal 302 goes from high to low and

signal 301 is low, decrement mode is selected enabling the resistance to decrease. When signal 302 goes from high to low and signal 301 is high, increment mode is selected enabling resistance to increase.

[00045] Digital pot 208 is set in an increment or decrement mode depending on whether it is configured as a potentiometer or a variable resistor.

[00046] Thereafter, pin 3 is toggled, which steps wiper 312, changing the resistance between pins 5 and 6. The goal is to reach a certain voltage divider output, Y volts (for example, 0.7Vdd) to enable writes to NVRAM 205 after power up and/or reset.

[00047] Assume that the range of the digital pot at resistance R is N steps. Each resistance step is R/N. Therefore, it will take X number of toggles to reach to voltage Y. If R is 50K-ohm, and N is 32, then it will take 15 toggles to reach 0.7Vdd.

[00048] The chances of random toggling of ASIC 200B control pins to enable the decrement mode (or increment mode if digital pot 208 is configured as a potentiometer) of digital pot 208, then toggle the UP/DN pin 15 times while remaining in decrement mode, is very small, and this minimizes the chances of NVRAM from getting corrupted at power up and/or reset.

[00049] Figure 4 shows a flow diagram of executable process steps for preventing corruption of an NVRAM, according to one aspect of the present invention. Turning in detail to Figure 4, in step S400, system 200B is powered up and/or reset.

[00050] In step S401, digital pot 208 is set to a certain resistance value. In the foregoing example, and in one aspect of the present invention, digital pot 208 is set around the mid-point of its resistance range.

[00051] In step S402, digital pot 208 is set in a decrement or increment mode. This is achieved by setting 301 low then bringing 302 from high to low (or when signal 302 goes from high to low and signal 301 is high for the increment mode).

[00052] In step S403, system 200B commands digital pot 208 to change the resistance between pins 5 and 6 by driving signals 301 and 302. To decrease the resistance, signal 301 is low and signal 302 is brought from high to low. Signal 301 is then toggled so that wiper 312 changes the resistance between pins 5 and 6.

[00053] In step S404, once the resistance between pins 5 and 6 is low, signal EE-PE 306 is enabled, which allows firmware of ASIC 200B to write to NVRAM 205, using signals 308-310.

[00054] In one aspect of the present invention, writing to NVRAM is disabled during power-up. Thereafter, writing to NVRAM is enabled. This minimizes the chances of accidental erasure during power up.

[00055] Although the present invention has been described with reference to specific embodiments, these embodiments are illustrative only and not limiting. Many other applications and embodiments of the present invention will be apparent in light of this disclosure and the following claims.